semiconductor regions flanking the trench gates on both of their sides and being in contact with said trench gates via films bordering and insulating the trench gates; and

a plurality of second semiconductor regions of the second conductivity type having a second depth as measured from said major surface of the body region that is less than the first depth,

wherein the second semiconductor regions connect the plurality of first semiconductor regions spaced apart from one another.

3. (Amended) A semiconductor device according to claim 1, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-like configuration.

4. (Amended) A semiconductor device according to claim 1, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-shaped configuration.

6. (Amended) A semiconductor device according to claim 1, further comprising a wiring member connected to at least one of the plurality of trench gates.

10. (Amended) A semiconductor device according to claim 1, further comprising a wiring member connected to the body region and to the second semiconductor region.

13. (Amended) A process for producing a semiconductor device comprising:

forming a body region of a first conductivity type in a semiconductor substrate, the body region having a major surface opposite to the surface shared between the semiconductor substrate and the body region;

forming a plurality of trench gates extending through the body region;

forming a plurality of first semiconductor regions of a second conductivity type that is different from the first conductivity type, the first semiconductor regions having a first depth as measured from said major surface of the body region, at least a portion of the first semiconductor regions flanking the trench gates on both of their sides and being in contact with said trench gates via films bordering and insulating the trench gates;

forming a plurality of second semiconductor regions of the second conductivity type having a second depth as measured from said major surface of the body region that is less than the first depth; and

connecting the plurality of first semiconductor regions spaced apart from one another by the second semiconductor regions.

15. (Amended) A process according to claim 13, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-like configuration.

16. (Amended) A process according to claim 13, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-shaped configuration.

Please see the attached Appendix for the changes made to effect the above claims.

IN THE ABSTRACT:

Please replace the abstract of the Disclosure with the Abstract provided on a separate page as required.

Please see the attached appendix for the changes made to effect the Abstract.